Page 1 of 12

Title: Applicants: Appl. No.: Filing Date: Express Mail No .: Detecting Over Programmed Memory After Further Programming
Chen, et al. Docket No.: SAND-01009US0 Unknown July 29, 2003 EV 332 013 508 US

Atty: Phone:

Fig. 1

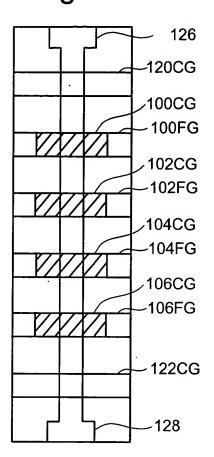


Fig. 2

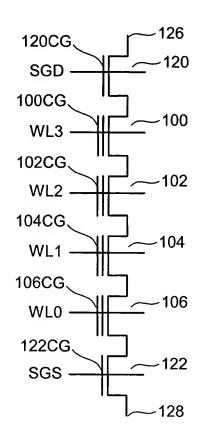
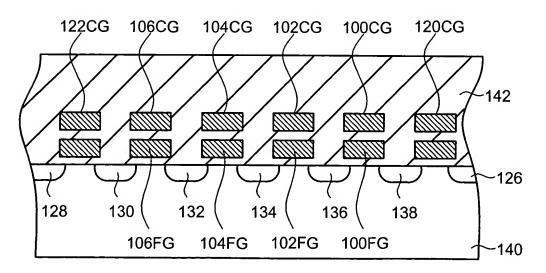


Fig. 3

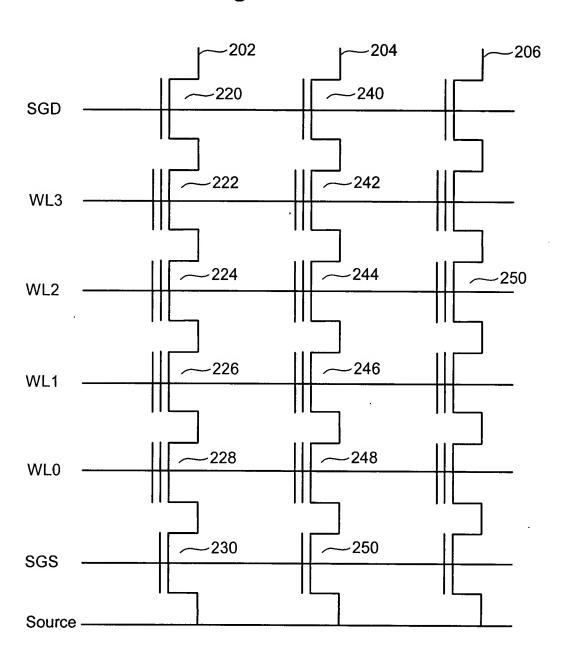


Page 2 of 12

Title: Applicants: Appl. No.: Filing Date: Express Mail No.: Detecting Over Programmed Memory After Further Programming
Chen, et al.
Docket No.: SAND-01009US0
Unknown Atty: Burt Magen July 29, 2003 EV 332 013 508 US

Phone:

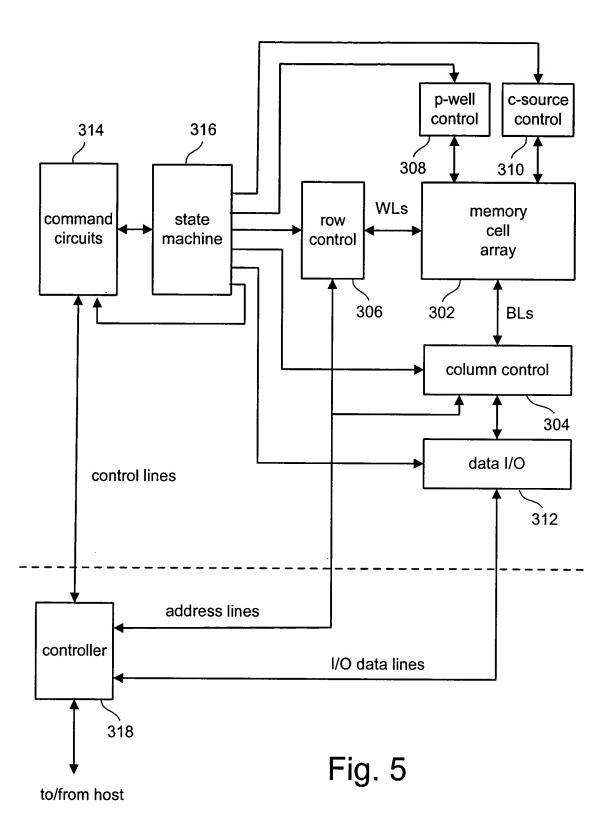
Fig. 4



Page 3 of 12

Title: Applicants: Appl. No.: Filing Date: Express Mail No.: Detecting Over Programmed Memory After Further Programming
Chen, et al. Docket No.: SAND-01009US0 Unknown July 29, 2003 EV 332 013 508 US

Atty: Phone:



Page 4 of 12

Title: Applicants: Appl. No.: Filing Date: Express Mail No.:

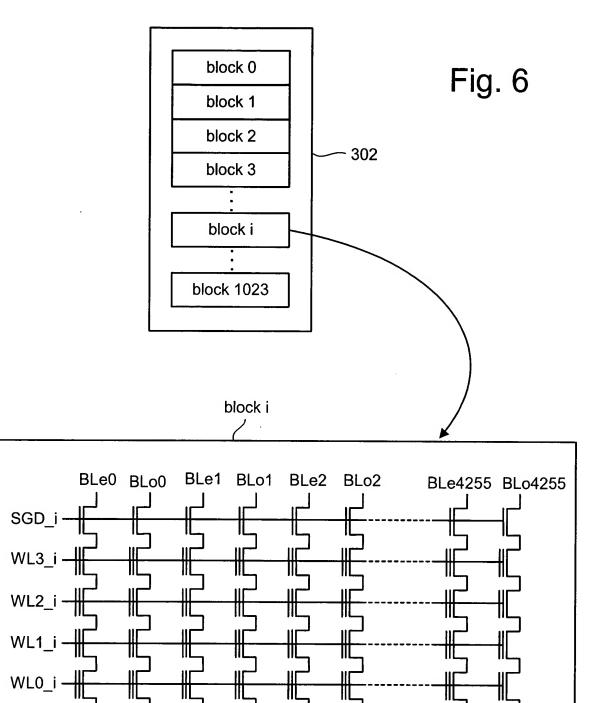
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Detecting Over Programmed Memory After Further Programming
Chen et al. Docket No.: SAND-01009US0 July 29, 2003 EV 332 013 508 US

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Page 5 of 12

Title: Applicants: Appl. No.: Filing Date: Express Mail No.: Detecting Over Programmed Memory After Further Programming
Chen, et al.
Docket No.: SAND-01009US0
Unknown Atty: Burt Magen July 29, 2003 EV 332 013 508 US

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(415) 369-9660

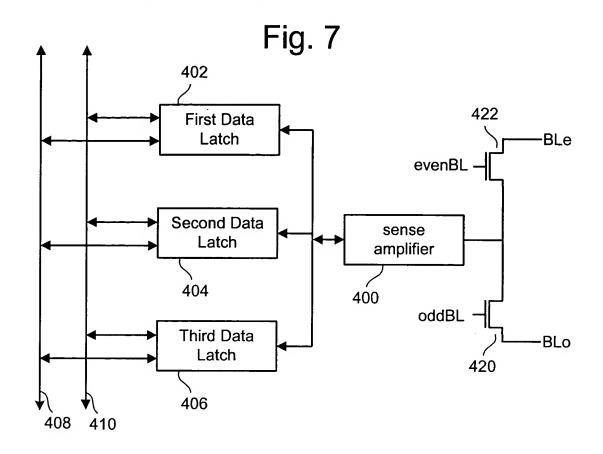
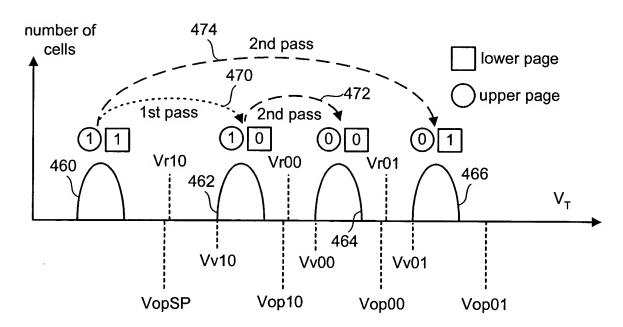


Fig. 8

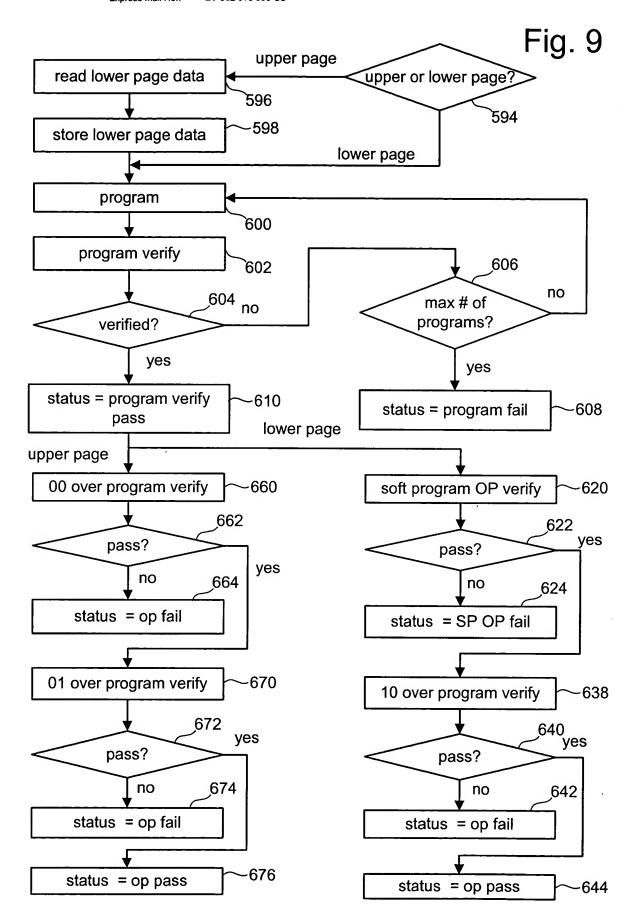


Page 6 of 12

Title: Applicants: Appl. No.: Filing Date: Express Mail No.: Detecting Over Programmed Memory After Further Programming

Other Office And Docket No.: SAND-01009US0 Unknown July 29, 2003 EV 332 013 508 US

Atty: Phone:

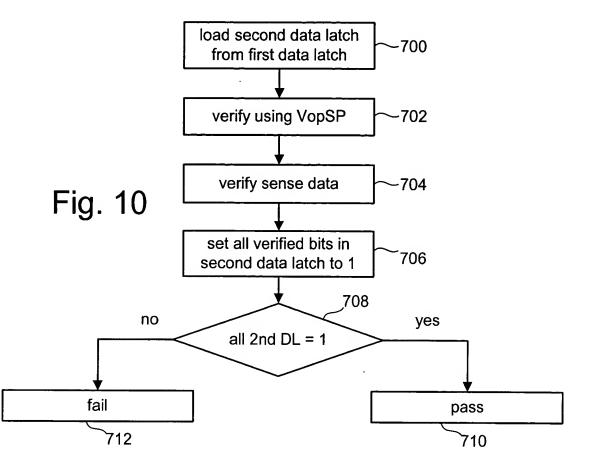


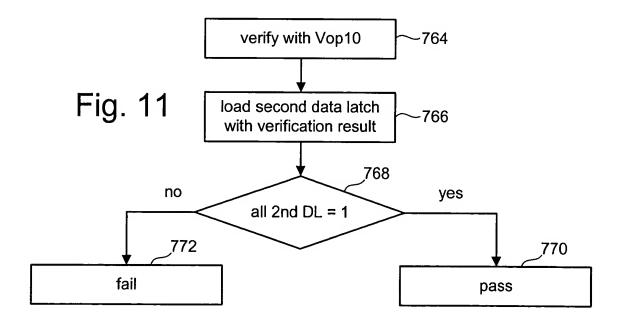
Page 7 of 12

Title: Applicants: Appl. No.: Filing Date: Express Mail No.: Detecting Over Programmed Memory After Further Programming Chen, et al. Docket No.: SAND-Unknown July 29, 2003 EV 332 013 508 US

Phone:

SAND-01009US0 Burt Magen (415) 369-9660

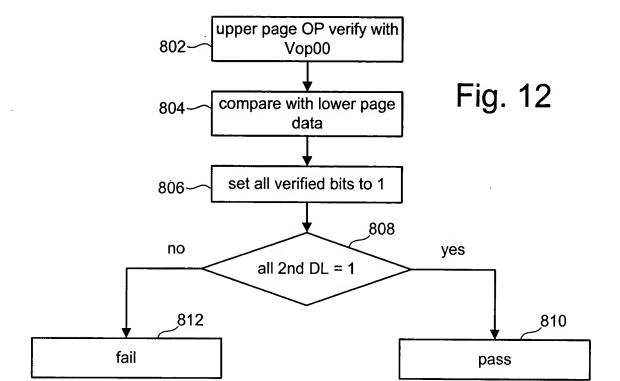


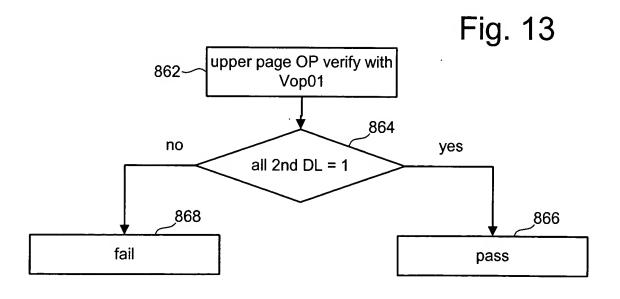


Page 8 of 12

Title: Applicants: Appl. No.: Filing Date: Express Mail No.: Detecting Over Programmed Memory After Further Programming
Chen, et al. Docket No.: SAND-01009US0 Unknown July 29, 2003 EV 332 013 508 US

Phone:



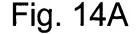


Page 9 of 12

Applicants: Appl. No.: Filing Date: Express Mail No .: Detecting Over Programmed Memory After Further Programming Chen, et al. Unknown July 29, 2003 EV 332 013 508 US

Docket No.: Phone:

SAND-01009US0 Burt Magen (415) 369-9660



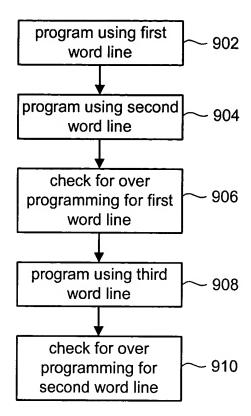
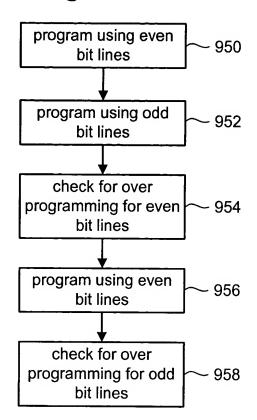
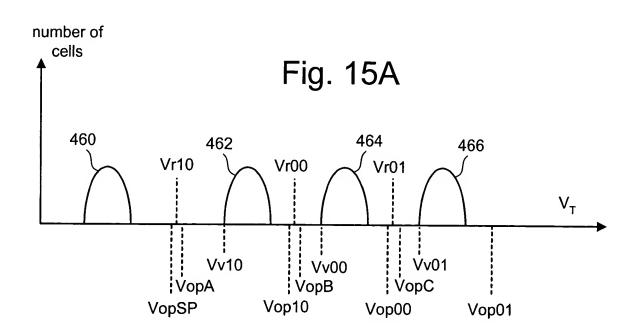


Fig. 14B



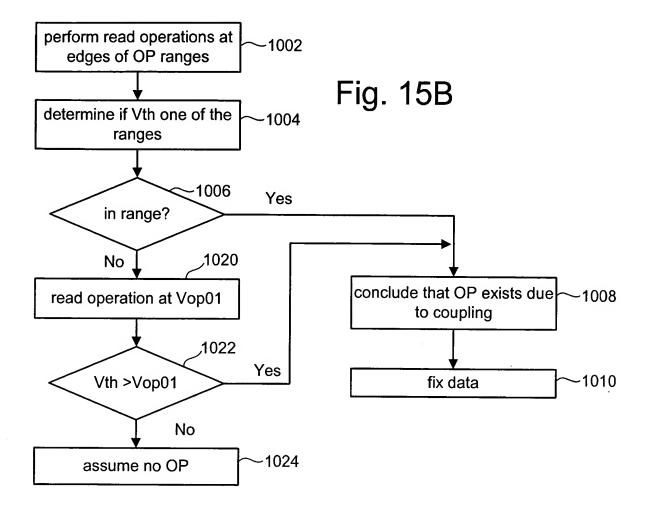


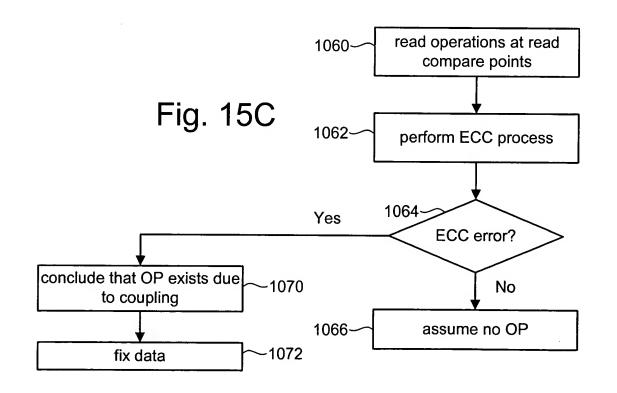
Page 10 of 12

Title: Applicants: Appl. No.: Filing Date: Express Mail No.: Detecting Over Programmed Memory After Further Programming Chen, et al. Unknown July 29, 2003 EV 332 013 508 US

Docket No.: Atty: Phone:

SAND-01009US0 Burt Magen (415) 369-9660





Page 11 of 12

Title: Applicants: Appl. No.: Filing Date: Express Mail No.: Detecting Over Programmed Memory After Further Programming
Chen, et al. Docket No.: SAND-01009US0 Unknown July 29, 2003 EV 332 013 508 US

Atty: Phone:

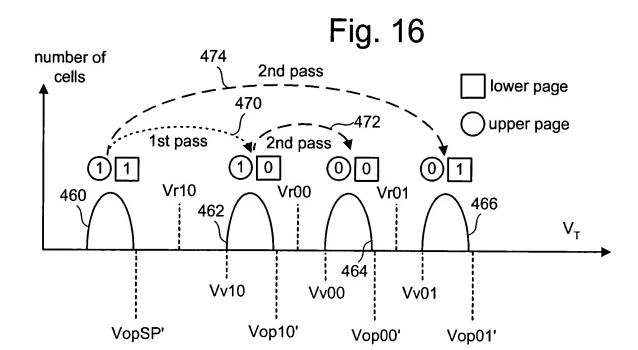


Fig. 17

	1	0
Read at VopSP'	1/0	0
Second Data Latch	1/0	0
First Data Latch	1	0
Test	Pass/Fail	Pass

Fig. 18

	11	10	00	01
Read at VopSP'	1/0	0	0	0
Second Data Latch	1/0	0	0	0
Third Data Latch	1	0	0	0
Test	Pass/Fail	Pass	Pass	Pass

Page 12 of 12

Detecting Over Programmed Memory After Further Programming
Chen, et al. Docket No.: SAND-01009US0

Applicants: Appl. No.: Filing Date:

Unknown July 29, 2003

Atty: Phone:

Burt Magen (415) 369-9660

Express Mail No.:

EV 332 013 508 US

Fig. 19

	1	0
Read at Vop10'	1	1/0
Second Data Latch	1	1/0
First Data Latch	1	0
Test	Pass	Pass/Fail

Fig. 20

	11	10	00	01
Read at Vop10'	1	1/0	0	0
Second Data Latch	1	1/0	0	0
First Data Latch	1	1	0	0
Test	Pass	Pass/Fail	Pass	Pass

Fig. 21

	11	10	00	01
Read at Vop00'	1	1	1/0	0
Second Data Latch	1	1	1/0	0
Third Data Latch	1	0	0	1
Test	Pass	Pass	Pass/Fail	Pass

Fig. 22

	11	10	00	01
Read at Vop01'	1	1	1	1/0
Second Data Latch	1	1	1	1/0
Test	Pass	Pass	Pass	Pass/Fail